РАДІОТЕХНІКА ТА ТЕЛЕКОМУНІКАЦІЇ

UDC 621.317.32
DOI https://doi.org/10.32782/2663-5941/2023.6/03

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DIGITAL POTENTIOMETER-CONTROLLED PROGRAMMABLE INSTRUMENTATION AMPLIFIER

The subject matter of the article concerns the schematic designs of instrumentation amplifiers with programmable gains, specifically tailored for digital processing and mixed-signal, measuring instruments, and data analysis systems. The central goal is to design a circuit that efficiently integrates the advantages of existing programmable instrumentation amplifiers, while also offering the capability to adjust the gain through a digital I2C/SPI interface. The research tasks comprised the analysis of current implementations of instrumentation amplifiers with programmable gains, focusing on their inherent strengths and limitations. This analysis was further extended to describe the operational principle of the proposed amplifier, emphasizing the role of the digital potentiometer in setting the gain. The development of a calculation methodology specific to this amplifier and computer simulations of the proposed design were also undertaken to compare its performance against traditional fixed-gain amplifiers. The methods employed in this research incorporated comparative analysis, computer simulations of the proposed schematic solutions, and the formulation of mathematical models for the electronic components used. As per the results, a novel circuit solution was proposed for a compact programmable instrumentation amplifier, which is based on a differential amplifier with a fixed gain, augmented by a programmable digital potentiometer. This proposed solution was evaluated against existing solutions, and calculation method was introduced to calculate the specific parameters of such an amplifier. In conclusions, elements of the calculation method for the programmable amplifier were delineated, facilitating estimations of permissible input voltage levels and discreteness of gain adjustments. The proposed circuit solution exhibits several advantages, such as compactness, adaptability, an extensive gain range, and the ability for automatic gain error calibration. However, a notable limitation is the potential reduction in the common-mode rejection ratio at higher frequencies, attributed to the parasitic capacitance at the gain adjustment input pins.

Key words: *instrumentation amplifier, programmable amplifier, digital potentiometer, data collection systems, Inter-Integrated Circuit (I2C), Serial Peripheral Interface (SPI), programmable gain.*

Introduction and Problem Statement. In the rapidly evolving field of electronic systems, the accurate and efficient digital processing of analog signals has emerged as a critical requirement. Such a need arises from the frequently encountered challenge where the inherent level of analog signals is insufficient for leveraging the full range of the analog-to-digital converter (ADC). This inadequacy can lead to suboptimal data acquisition, especially when the input signals are of paramount importance. Specifically, in scenarios characterized by feeble signals amidst high interference, instrumentation amplifiers are frequently employed [1]. Their merits, ranging from the simultaneous setting of the necessary gain and offset to their substantial attenuation of common-mode noise and their ease of implementation, make them indispensable in various electronic systems. Nevertheless, a recurring and significant challenge with these amplifiers, particularly in systems demanding wide dynamic ranges, is their inherent fixed gain structure. The voltage at the output of the instrumentation amplifier is defined as:

$$V_{out} = G \cdot (V_p - V_n) + V_{ref} \quad (1)$$

Where G represents the predetermined gain, V_p is the voltage measured at the non-inverting input, V_n denotes the voltage at the inverting input, and V_{ref} stands for the bias voltage.

Addressing this limitation, this paper presents a new approach towards the design of programmable

instrumentation amplifiers. By combining the benefits of existing programmable instrumentation amplifiers, the proposed design further pioneers the incorporation of a digital interface, specifically the I2C/SPI, to provide a much-desired capability: the adjustment of amplifier gain via digital interface. Such feature can be used in many fields, like environmental sensors pre-processing [2], radiometric measurements [3], etc. To establish the foundation of this research, a comprehensive analysis of the current landscape of programmable gain instrumentation amplifiers was conducted, analyzing their strengths and potential areas of improvement.

One prevalent method for constructing programmable gain amplifiers (PGAs) involves utilizing electromechanical relays. These components, directed by the measurement module, implements the connection of gain-setting resistors (R1-R4) with predetermined values to the integrated instrumentation amplifier (Fig. 1).

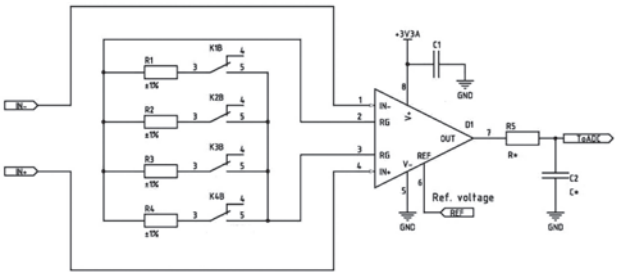

Fig. 1. Variable gain instrumentation amplifier with gain control based on electromechanical relays

This approach offers several benefits, including a minimal impact on the amplifier's frequency response, precise gain configuration, straightforward implementation, and a versatile and scalable system [4]. Consequently, this technique is used in the analog front-end modules of precision measurement apparatuses, particularly in scenarios where larger sizes, higher implementation costs, and susceptibility to mechanical stress do not pose considerable drawbacks.

However, it is important to note the limitations of this system, such as a restricted range of attainable gain values, necessitating an individual relay for each distinct gain. A possible substitute for the electromechanical relay is the employment of multi-channel analog switches [5] (Fig. 2).

While these switches offer numerous advantages, including rapid switching capabilities, compactness, and robustness against mechanical disturbances, they also introduce certain imperfections. Notable among these are the considerable non-linear resistance intrinsic to the switches, their larger footprint relative to digital potentiometers, and elevated output capacitance in switches with minimal resistance (ranging from several to hundreds of picofarads). The latter detrimentally impacts the common-mode noise rejection ratio (CMRR), besides the relatively high expense for switches with favorable specifications [6]. Furthermore, the challenge of establishing additional gain values persists, given that most analog switch producers manufacture units with a ceiling of 4–8 channels, occasionally failing to meet the requisite quantity of gain variations.

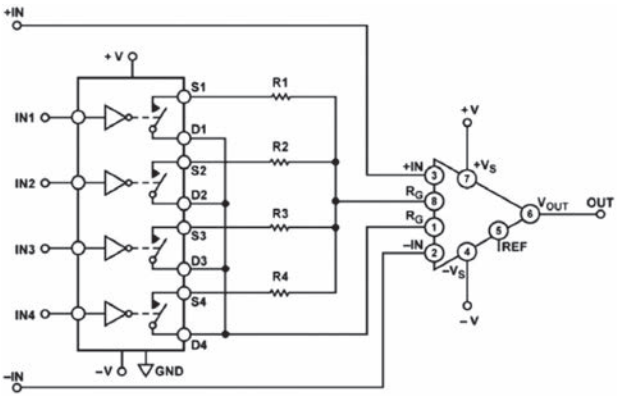

Fig. 2. Variable gain instrumentation amplifier with gain control based on analog switch

In this context, it is also pertinent to note the AD825x and AD8231 series of integrated programmable instrumentation amplifiers, developed by Analog Devices [7]. Although these amplifiers largely circumvent the deficiencies, they impose constraints on engineers by precluding the custom selection of essential gain values and intrinsic parameters of the instrumentation amplifier. This lack of flexibility could be a limiting factor in certain specialized or nuanced applications.

However, the recent advancements in the programmable-gain amplifiers domain have been driven by the need for low-power consumption, high bandwidth, and precise gain control.

Analysis of recent research and publications. Park et al. (2023) conducted research on decibel-linear PGAs and presented a new design using the complementary current-switching approach. This innovative design offers a more expansive bandwidth and a significant gain control capability, and it efficiently reduces DC power usage. Utilizing a 65-nm CMOS process, their PGA demonstrated a dB-linear gain control range of 59.7 dB in 1-dB increments, consuming only 0.6 mW of DC power [8].

In the automotive sector, ultrasonic sensor systems have gained traction, necessitating specialized PGAs. Addressing this need, Kang et al. (2023) pro-

posed a PGA that adeptly removes DC offset and out-of-band noise through band-pass filtering. Their design intricately combines a low-noise amplifier (LNA), a variable gain amplifier (VGA), an RC low-pass filter (LPF), and a voltage buffer. Notably, the PGA's voltage gain can be fine-tuned from 56 dB to 110 dB within the ultrasonic signal band spanning from 30 kHz to 70 kHz [9].

Shifting focus to CMOS technology, Germano et al. (2023) presented a dynamic residue amplifier in 65 nm CMOS, tailored for a 2-stage SAR-pipelined ADC. Their design stands out for its programmable gain, achieved by varying both the common-mode current and the amplification time window. Post-layout simulations across different conditions revealed a configurable gain with a power consumption range between 39-61 μW [10].

Kledrowetz et al. (2023) made research in the domain of EMG sensor signal processing, introducing an analog front-end powered by a mere 1 V. Their design, realized using the 28 nm fully depleted silicon on insulator (FDSOI) technology, comprises an input instrumentation amplifier (INA) and a PGA, both in a fully differential topology. This circuit achieves a commendable common-mode rejection ratio (CMRR) of 105.5 dB [11].

Lastly, in the field of wearable ECG sensors Kumar and Balanethiram (2023) proposed an Analog Front End (AFE) that is DC coupled, integrating an FDDA-based Instrumentation Amplifier (IA) and a PGA with an AC coupled input stage. This design is particularly noteworthy for its high gain of 76dB and a CMRR of around 127dB, making it adept at detecting ECG signals in the range of 1-2 millivolt peak to peak [12].

However, a critical examination of these advancements reveals a common thread that poses a significant limitation: each of these innovative PGAs relies heavily on CMOS technology for their implementation. Such features allowed researchers to achieve the micro-scale dimensions and the low power consumption inherent in CMOS-based designs. While these characteristics are advantageous in certain applications, they present a considerable barrier when these PGAs are considered for environments that require or favor discrete component implementation.

The constraint lies in the infeasibility of directly translating these sophisticated, complicated, miniaturized CMOS designs into the macro-scale world of discrete components. Discrete implementation, with its own set of advantages, including lower initial expenses, ease of debugging and implementation, modification upon required tasks, and unique educational value, is virtually sidelined by the current research trajectory focused predominantly on CMOS technology. This gap in research inclusivity underscores the need for a paradigm shift, prompting a move towards designs that embrace the versatility and accessibility of discrete components.

Task statement. The research tasks comprised the analysis of current implementations of instrumentation amplifiers with programmable gains, focusing on their inherent strengths and limitations. This analysis was further extended to describe the operational principle of the proposed amplifier with a digital potentiometer-controlled gain. The development of a calculation methodology specific to this amplifier and computer simulations of the proposed design also will be undertaken to compare its performance against traditional fixed-gain amplifiers. Performance testing will primarily be executed through computer simulations, which will allow us to compare our new design with traditional fixed-gain amplifiers. These simulations are crucial for validating our design and making necessary adjustments to enhance its performance.

Outline of the main material of the study. In our goal of modeling a programmable differential amplifier, the first step is the calculation of the circuit's maximum and minimum potential gains. This is achieved using the equation (2):

$$1+\frac{49400}{R_{ab}}<G<1+\frac{49400}{R_{aw\min}}$$
$$2<G<1412 \quad (2)$$

where R_{ab} denotes the maximum resistance the digital potentiometer can offer, which is 50 kOhm in the current context. R_{awmin} corresponds to the resistance of the potentiometer's middle terminal, essentially setting the minimum resistance for the digital potentiometer. For the models AD5272 / AD5274, this resistance approximates to 35 Ohm. The constant 49400 references the internal gain-set resistor intrinsic to the AD8226 amplifier. It is pertinent to note that the maximum and minimum gain values are also constrained by the specifications of the instrumentation amplifier. Specifically, for the AD8226, the permissible gain should be between 1 and 1000. Given that we are employing the AD5272BRMZ-50-RL7 potentiometer, the gain range extends from a minimum of 2 to a maximum limited by the amplifier, 1000. Consequently, incorporating a digital potentiometer effectively taps into most of the accessible gain range delivered by the instrumentation amplifier.

$$G\le 1+\frac{148.2}{V_{in}} \quad (3)$$

Equation (3) clarifies the relationship between permissible gain and the differential voltage at the

input. This equation was derived by substituting R_{ab} with $V_{in}/3mA$, where $3mA$ denotes the maximum current, the digital potentiometer can handle.

$$G \le 1 + \frac{49400}{D \cdot \frac{R_{ab}}{2^N}} \quad (4)$$

Equation (4) showcases the interdependence of gain on the binary code set in the digital potentiometer. Here, D represents the binary code fed into the potentiometer, R_{ab} symbolizes the potentiometer's nominal resistance, and N stands for the potentiometer's resolution, which is 10-bit in the present context.

Fig. 3 illustrates the correlation between the peak permissible gain and the input voltage. The amplifier's input differential voltage has an upper limit set by the AD5272BRMZ's peak taper current (3mA).

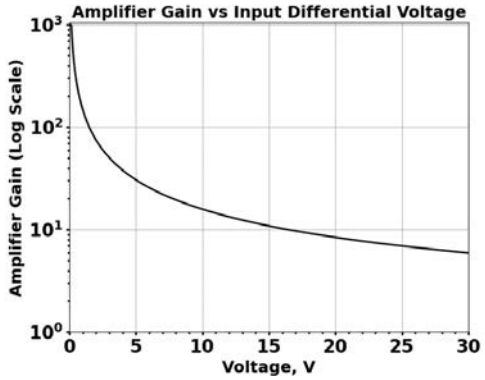

Fig. 3. Dependence of the maximum allowable gain over the input differential voltage

The graphical representation in Fig. 4 emphasizes that the amplifier, within high gain parameters, proffers a diminished granularity in gain adjustment (yielding larger gain intervals). Conversely, in lower gain ranges, the resolution increases. This characteristic is inherently advantageous in practical scenarios, facilitating precision gain adjustment where it's most requisitioned.

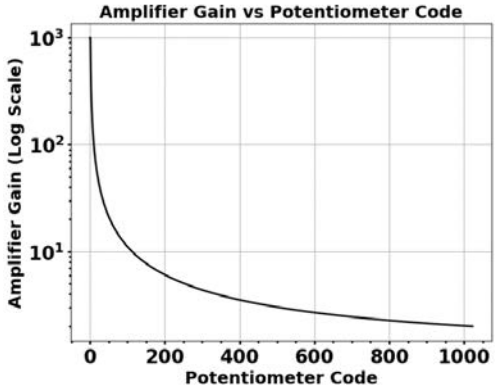

Fig. 4. Dependence of the gain over the binary code specified in the potentiometer

Fig. 5 represents the common mode noise rejection ratio (CMRR) of the amplifier versus the input frequency, comparing both a digital potentiometer (DigiPOT) and a conventional discrete resistor setup. This data was procured using SPICE simulations. A minor dip in the CMRR of the amplifier with a potentiometer at elevated frequencies is attributable to the intrinsic parasitic capacitance present at the gain inputs. Nonetheless, it's vital to underscore that combining analog and digital modules in a single circuit configuration is a prevalent endeavor. Adhering to generally accepted circuit design and routing rules ensures that performance degradation remains negligible [13].

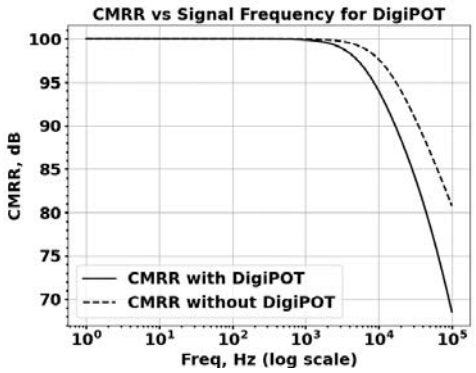

Fig. 5. Dependence of the common mode noise rejection ratio over the frequency of the input signal

Fig. 6 illustrates the proposed amplifier design, developed with a focus on optimizing the Bill of Materials (BOM) for cost-effectiveness, ensuring versatility, and facilitating seamless integration with the Analog-to-Digital Converters (ADCs) inherent in various microcontrollers.

The operational sequence commences with the differential input signal being applied to the IN+ and IN- terminals. This signal is subsequently subjected to an RF interference suppression stage and an input protection mechanism, important for protecting the amplifier's inputs. It is critical that the passive components' values are selected aligning with the operational demands of the specific electronic application to ensure signal integrity and reliability.

After the input conditioning, the signal is routed to the differential amplifier, designated as D2 in the schematic. Here, gain setup is accomplished through the integration of a programmable digital potentiometer D1, providing control over the amplification, while ensuring optimal signal-to-noise ratio (SNR) and minimal harmonic distortion.

In the core amplification stage, the AD8226 instrumentation amplifier from Analog Devices is used

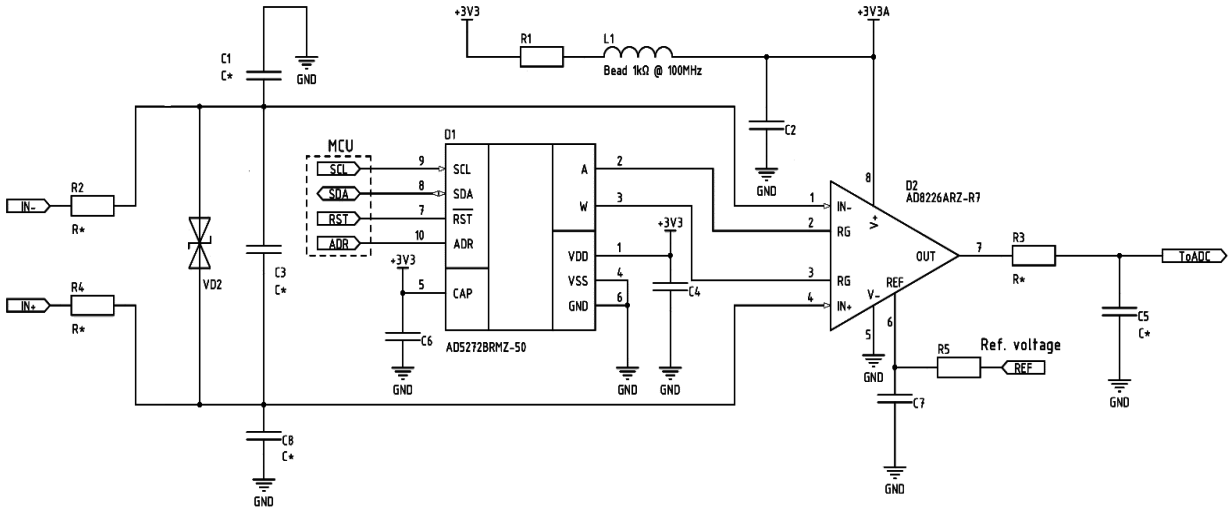

Fig. 6. Dependence of the common mode noise rejection ratio over the frequency of the input signal

[14]. To mitigate power supply noise – detrimental to the low-level signal integrity – a decoupling network comprising R1-L1-C2 is implemented. This configuration decisively isolates the digital circuitry from the analog domain, substantially reducing parasitic interference and ensuring optimal power delivery to the critical operational stages.

Utilizing the AD5272 digital potentiometer from Analog Devices [15], the design achieves up to 1024 distinct resistance configurations, broadening the dynamic range and allowing for accurate signal scaling. The biasing filter (R5-C7), provides the reference voltage to the amplifier's REF input, ensuring stable operation across varying environmental conditions and operational demands.

This reference voltage, crucial for accurate signal processing, can be derived from a buffered resistor divider network or a microcontroller-integrated Digital-to-Analog Converter (DAC), enhancing system versatility and adaptive biasing capabilities. This approach facilitates real-time, software-driven offset calibration, optimizing measurement accuracy and system responsiveness.

In the final signal conditioning stage, the amplified output undergoes a low-pass filter (R3-C5), attenuating high-frequency signal artifacts and ensuring spectral purity before ADC interfacing. The signal is then sent to the microcontroller's ADC module for high-resolution digital conversion, enabling digital signal processing techniques or subsequent routing to external analytic instrumentation. This design yields a system characterized by its precision, configurability, and seamless integration into broader electronic architectures.

Conclusions. In this study, we presented a novel approach to design programmable differential amplifiers. A thorough evaluation of the merits and demerits of this methodology was undertaken.

The salient features of the introduced differential amplifier encompass its compact footprint, customizable parameters, extensive gain variability, potential for automated gain error calibration, affordability, and straightforwardness in both fabrication and integration. On the flip side, certain limitations were observed. These include a minor dip in the Common Mode Rejection Ratio (CMRR) of the instrumentation amplifier at higher frequencies, attributable to the inherent parasitic capacitance at the gain setting inputs [16]. Additionally, the bandwidth is restricted by the characteristics of the digital potentiometer.

Throughout this research, we delineated computational techniques tailored for our suggested programmable instrumentation amplifier. These computations facilitate estimations of permissible input voltage thresholds and the discreteness of gain adjustments.

The proposed circuit design allows the development of compact, low-power, robust mixed-signal devices, biomedical instruments, systems dedicated to quantifying physical parameters, systems for collecting novel design facilitates a broad gain range controlled digitally, introducing substantial improvements in adaptability and precision for various applications. While the model exhibits enhanced functionality, particularly in automated gain calibration and error reduction, it encounters constraints in high-frequency common-mode rejection ratio (CMRR) due to inherent parasitic capacitance. Nonetheless, the proposed PIA stands as an important advancement, offering notable benefits for digital processing systems, biomedical instrumentation, and diverse measurement devices requiring dynamic and accurate signal amplification. Future research should investigate methods to mitigate the high-frequency limitations to further solidify the proposed PIA's applicability in more complex or high-frequency reliant systems.

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Бурковський Я.Ю., Зіньковський Ю.Ф. ПРОГРАМОВАНИЙ ІНСТРУМЕНТАЛЬНИЙ ПІДСИЛЮВАЧ З ВСТАНОВЛЕННЯМ ПОСИЛЕННЯ ЗА ДОПОМОГОЮ ЦИФРОВОГО ПОТЕНЦІОМЕТРА

Предметом вивчення в статті є схемотехнічні рішення інструментальних підсилювачів з програмованим коефіцієнтом підсилення (programmable gain instrumentation amplifiers) для вирішення прикладних завдань в системах цифрової обробки аналогових сигналів, біомедичної апаратури, вимірювальних приладах, аналізі даних з аналогових датчиків і т.д. Метою є розробка схемотехнічної реалізації програмованого інструментального підсилювача, що об'єднує переваги вже відомих рішень з

можливістю завдання необхідного значення посилення по цифровому інтерфейсу I2C / SPI. Задачі: провести аналіз існуючих реалізацій інструментальних підсилювачів з програмованим коефіцієнтом підсилення з урахуванням їх переваг і недоліків; описати принцип роботи запропонованої реалізації програмованого інструментального підсилювача з цифровим потенціометром в якості елемента, що задає значення посилення; створення деяких елементів методики розрахунку подібного підсилювача; проведення комп'ютерного моделювання запропонованого рішення і порівняння отриманих результатів з такими у реалізації інструментального підсилювача з фіксованим коефіцієнтом посилення. Використовуваними методами є: порівняльний аналіз як метод дослідження, комп'ютерне моделювання схемотехнічних рішень, математичне моделювання. Отримані наступні результати. В ході роботи було запропоновано нове схемотехнічне рішення малогабаритного програмованого інструментального підсилювача, проведено його порівняння з уже існуючими реалізаціями, запропонована методика розрахунку параметрів такого інструментального підсилювача, а також показані результати комп'ютерного моделювання. Проведено оцінку переваг і недоліків. Проведений аналіз запропонованої реалізації програмованого інструментального підсилювача дозволяє зробити висновки, що до переваг можна віднести малі розміри готового рішення, можливість зміни під необхідні параметри, максимально можливий діапазон регулювання посилення, можливість автоматичного калібрування похибки установки посилення, невисоку вартість реалізації (в порівнянні з іншими, представленими в статті методами) і відносну простоту реалізації. До недоліків можна віднести деяке зниження коефіцієнта подавлення синфазної завади інструментального підсилювача на високих частотах через паразитні ємності на входах установки посилення.

Ключові слова: *інструментальний підсилювач, програмований підсилювач, цифровий потенціометр, системи збору даних, Inter-Integrated Circuit (I2C), Serial Peripheral Interface (SPI), програмоване посилення.*